Kagawa teaches a high frequency, high power transistor in which the impedance of the bond wires is important, but not related to the performance characteristics of the transistor *after* the die is secured to the substrate

Nishiuma discloses using a bond wire in close proximity to a ground plane separated by a dielectric to produce a transmission line which matches impedance of the input signal line by selecting the thickness of the dielectric and the dielectric constant of the material.

Even if it were proper to combine the high power transistor of Kagawa with the transmission line of Nishiuma, and Applicants do not concede that it is, such a combination does not teach or suggest the "impedance setting" methods of claims 1 and 5, or circuits constructed by such impedance setting methods recited in claims 9 and 13.

In addition, neither Kagawa nor Nishiuma provides motivation for, or even suggests such a combination, especially *after the transistor die is secured to the substrate.* Nor does the Examiner separately provide the source of such motivation.

More particularly, Kagawa teaches that "wires 25 and 26 have equal lengths and are symmetrical (in the vertical direction in the drawing) relative to the transistor cells 6 interposed therebetween" (column 4, lines 35-38). The underlying assumption is that each transistor (cell) has uniform performance characteristics (col. 4, lines 43-46) and can be accurately characterized without post die attach testing, and adequately compensated with uniform and symmetrical circuits (col. 4, lines 38-43).

This is completely opposite to the methods of claims 1 [and 5], which each recite, inter alia:

securing a die to a substrate, the die comprising a transistor having an input [output] terminal;

measuring a performance characteristic of the transistor;

using one or more wires to electrically couple the transistor input terminal to an input [output] matching element, an input [output] signal lead, or both; and

setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic.

Notably, individual transistor performance characteristics vary, as stated in the application on page 2, lines 16-17: "These variances must be compensated for in the amplification circuits to achieve reliable and consistent performance". Such variations in transistor performance characteristics occur at the output in much the same way as the input. In accordance with the methods of claims 1 and 5, the impedance of one or more bond wires is set (e.g., determined by length and/or number of bond wires), at least in part on the measured transistor performance characteristic. The circuits of claims 9 and 13 are constructed in accordance with the respective claimed impedance setting methods of claims 1 and 5.

Nishiuma, based on the abstract provided by the Examiner, teaches producing a bond wire transmission line with a characteristic impedance that matches the impedance (50 ohms) of the input signal line 7. This is to prevent reflection of the input signal at the junction between the input signal line 7 and the bond wire 9. There is no suggestion of an impedance transformation network to match the 50 ohm input signal impedance to the relatively lower input impedance of the transistor, or any other transistor performance

characteristics. Further, there is no motivation or suggestion that the number or length of the bond wires be adjusted to achieve a 50 ohm match: rather the distance between the wire and the ground plane, and the dielectric thickness and relative "permittivity" are suitably selected.

For the above reasons, applicants respectfully request withdrawal of the claim rejections, including for the same reasons the rejection of the dependent claims 2-4, 6-8, 10-12 and 14-16.

**Conclusion**

In view of the above comments, allowance of the application is respectfully requested. If the Examiner has any questions regarding this paper or the application in general, he is invited to call the undersigned at the number listed below.

Respectfully submitted,

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Marked up version of the amended abstract:

A method for manufacturing a power transistor circuit includes securing a die to a substrate, the die comprising a transistor having an input terminal and an output terminal. One or more performance characteristics of the transistor are measured. Using one or more wire sets, the transistor input terminal is electrically connected to one or more input matching elements and an input signal lead. The impedance of the one or more wire sets, [()]as determined by selecting a desired number and/or length of the wires in each set, is selected based at least in part on the measured transistor performance characteristic(s). Similarly, using one or more additional wire sets, the transistor output terminal is electrically connected to one or more output matching elements and an output signal lead, wherein the impedance of the additional wire sets is selected based at least in part on the measured transistor performance characteristic(s).